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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,188	03/14/2001	Hiroshi Morioka	501.30598CC3	2601

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EXAMINER	
NGUYEN, TU T	

ART UNIT	PAPER NUMBER
2877	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/805,188	MORIOKA ET AL.	
	Examiner	Art Unit	
	Tu T. Nguyen	2877	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/535,577.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamoshida (4,571,685) in view of Koizumi et al (4,614,427) and Oshida et al (4,744,666) or Scheff et al (5,172,000).

With respect to claim 1, Kamoshida discloses a processing method for semiconductor devices in a semiconductor fabrication line, comprising the steps of: processing a substrate in a first processing apparatus (abstract), transferring the substrate processed in the first processing apparatus to a detecting apparatus without removal of the substrate from the semiconductor fabrication line while continuing fabrication of the semiconductor devices 79 (fig 9).

Kamoshida discloses a detecting apparatus. However, Kamoshida does not explicitly disclose a particle detecting apparatus. Koizumi discloses a system for detecting a foreign particles (columns 1-2). The system comprises: a detecting apparatus 35 (fig 3) and a particle detecting processing apparatus 61-62 (fig 3) which is separated from the detecting apparatus (fig 3), sending a detected signal to the particle detecting process apparatus (column 5, lines 30-40). It would have been obvious to

modify Kamoshida with Koizumi's particle detecting apparatus to increase yield as taught by Kamoshida in column 1, lines 35-42. Kamoshida discloses a CPU 100 (fig 9) for storing and transferring the data between the systems (column 4, lines 30-40). It would have been obvious to modify Kamoshida's computer system for storing the amount of the foreign particle defects for utilizing the testing.

Koizumi does not disclose a variable spatial filter as claimed. Oshida discloses a spatial filter which is variable according to a pattern of the wafer (abstract or column 2, lines 3-10). Scheff discloses the same spatial filter as claimed (abstract or figs 4,5). It would have been obvious to modify Koizumi's detecting apparatus with the spatial filter as taught by Oshida or Scheff for inspecting different wafer patterns as taught by Scheff in column 1, lines 45-55.

With respect to claims 2,5,23, since Koizumi discloses focusing an incident light in a spot on a wafer (column 3, lines 12-15), Koizumi inherently discloses detection is performed in a predetermined area of the substrate.

With respect to claim 3, Kamoshida does not explicitly disclose a processing time. However, the skill artisan would have been motivated to have a completed detecting step within a processing time in the processing step to be ready for transferring the information to the next step.

With respect to claims 4,26, refer to discussion in claim 1 above. Further, Kamoshida discloses controlling the processing step based on the information on the finishing product (column 4, lines 30-40). It would have been obvious to modify Kamoshida to control the operation of the semiconductor fabrication line in accordance with the data of foreign particle defects to increase the yield.

With respect to claim 6, refer to discussion in claim 1 above for detecting the particle defects. Further, Koizumi does not disclose counting the defects. Counting the defects on the wafer would have been known. It would have been obvious a design choice to modify Kamoshida's system to count the defects to give more detail about the condition of the wafer.

With respect to claim 7, refer to discussion in claim 1 for storing the data in the memory.

With respect to claim 8, refer to discussion in claim 1 above for detecting foreign particle. Further Kamoshida's detecting apparatus performs in a real time (columns 2-3).

With respect to claim 9, Since Koizumi discloses using a detector for detecting the particle, Koizumi inherently discloses the claimed invention.

With respect to claim 10, refer to discussion in claim 1.

With respect to claim 11, the skill artisan would have been motivated to modify Koizumi's system to output the signal indicating the condition of the wafer as claimed. The modification involves only routine skill in the art.

With respect to claims 12,17,22, refer to discussion in claim 1. Further, Koizumi discloses using a filter (column 1, lines 30-65) to cut a light reflected from a pattern formed on the substrate.

With respect to claim 13, refer to discussion in claim 1 above.

With respect to claims 14,19, Koizumi inherently discloses the claimed limitation.

With respect to claims 15-16,18,20-21, refer to discussion in claim 1.

With respect to claim 24, Koizumi does not explicitly disclose a linear image sensor. However, a linear image sensor would have been known. It would have been obvious to modify Koizumi with the known linear sensor to utilize the detection.

With respect to claim 25, Kamoshida does not explicitly disclose the first apparatus is an etching apparatus. However, it would have been obvious a design choice to have Kamoshida's first process as an etching apparatus.

With respect to claim 27, Koizumi does not explicitly disclose obtaining information of distribution of foreign particle defects. However, it would have been a design choice to modify Koizumi to manipulate the detected data for different purposes. The modification involves only routine skill in the art. Further, refer to discussion in claim 8 for the real time.

Response to Arguments

Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

With respect to Applicant's argument about the variable spatial filter, refer to discussion in claim above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu T. Nguyen whose telephone number is (571) 272-2424. The examiner can normally be reached on T-F 7:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu T. Nguyen
Primary Examiner
Art Unit 2877

03/20/2004